

4-bit DAC, Step-Down PWM Power Controller

■ FEATURE

- Compatible with HIP6008.
- Simple Voltage-Mode PWM Control.
- Fast Transient Response.
- $\pm 1.5\%$ 4-Bit Digital-to-Analog Output Voltage.
- Adjustable Current Limit without External Sense Resistors.
- Full 0% to 100% Duty Ratio.
- 200KHz Free-Running Oscillator, Programmable up to 350KHz.
- Power-Good Output Voltage Monitor.
- Short Circuit Protection with Low Short Circuit Output Current.
- TTL Compatible 4-bit Digital-to-Analog Core Output Voltage Selection, with range from 2.0V to 3.5V in 0.1V increments.

■ APPLICATIONS

- Power Supply for Pentium[®], Pentium Pro[®], Power PC[®] and Alpha[®] Microprocessors.
- High-Power 5V to 3.xV DC/DC Regulators.
- Low-Voltage Distributed Power Supplies.

■ DESCRIPTION

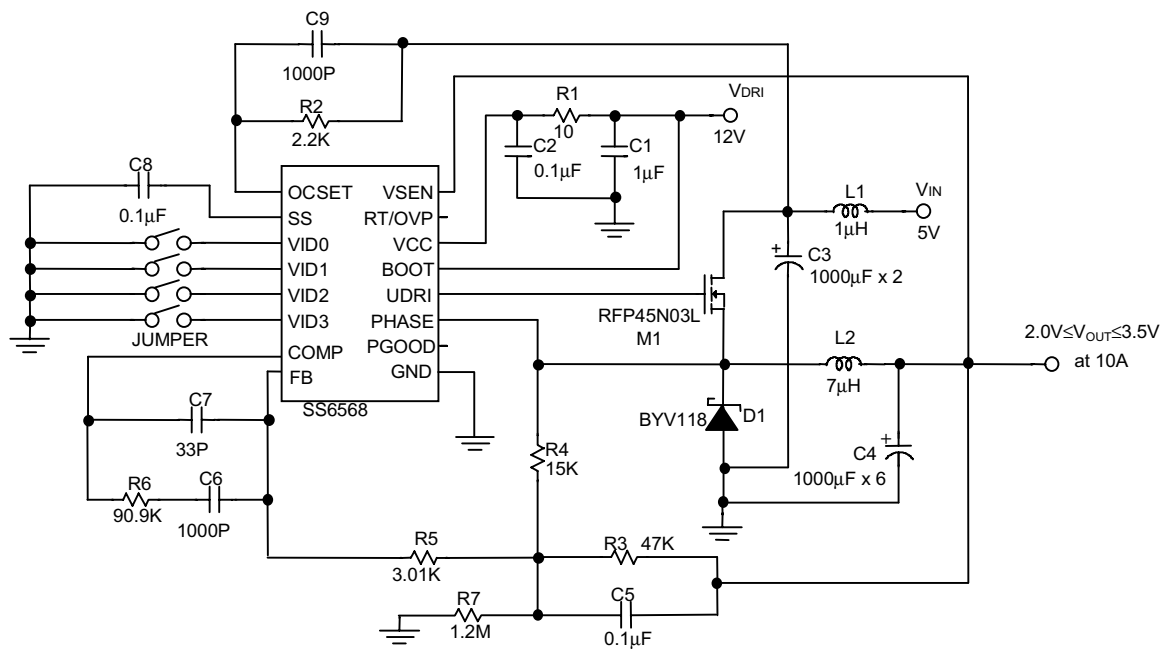
The SS6568 is a high power, high efficiency switching controller optimized for high performance microprocessor applications. It is designed to drive an N-channel MOSFET in a standard buck topology. Featuring a digitally programmable switching regulator, the SS6568 includes monitoring and protection capabilities in addition to all the essential PWM control functions.

The internal 4-bit Digital-to-Analog Converter (DAC) adjusts the output voltage from 2.0V to 3.5V in 0.1V increments. The precision reference and voltage-mode control can provide output regulation within $\pm 1.5\%$ over temperature and line voltage shifts.

The SS6568 includes an internal 200KHz free-running oscillator that can be adjusted up to 350KHz. The resulting PWM duty ratio ranges from 0% to 100%. The error amplifier features a 11MHz bandwidth and 6V/ μ S slew rate, which enables high converter bandwidth for fast transient response.

The SS6568 provides adjustable over current and short circuit protections. It senses the output current by using the $R_{DS(ON)}$ of the N-channel MOSFET without an external low value sense resistor. It also monitors the output voltage with a window comparator and issues a power good signal when the output is within 10% of the rated output voltage.

TYPICAL APPLICATION CIRCUIT



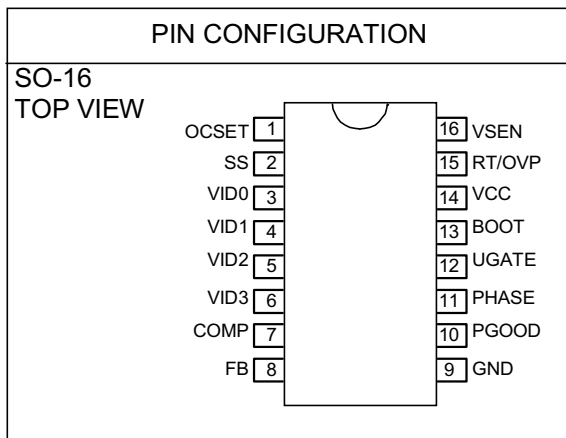
Switching DC/DC Converter

ORDERING INFORMATION

SS6568CXXX

- PACKING TYPE
TR: TAPE & REEL
TB: TUBE
- PACKAGING TYPE
S: SMALL OUTLINE

Example: SS6568CSTR
 → in SO-16 Package & Taping &
 Reel Packing Type



■ ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	15V
Boot Voltage, V_{BOOT}	15V
Input, Output, or I/O Voltage	GND - 0.3V to $V_{CC}+0.3V$
ESD Classification	Class 2

Recommended Operating Conditions

Supply Voltage, V_{CC}	12V±10%
Ambient Temperature Range	0°C ~ 70°C
Maximum Operating Junction Temperature	100°C

Thermal Information

Thermal Resistance, θ_{JA} (Typical, Note 1)	
SOIC Package	100°C/W
SOIC Package (with 3 in ² of Copper)	90°C/W
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C ~ 150°C
Maximum Lead Temperature (Soldering 10 Sec)	300°C

Note 1: θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

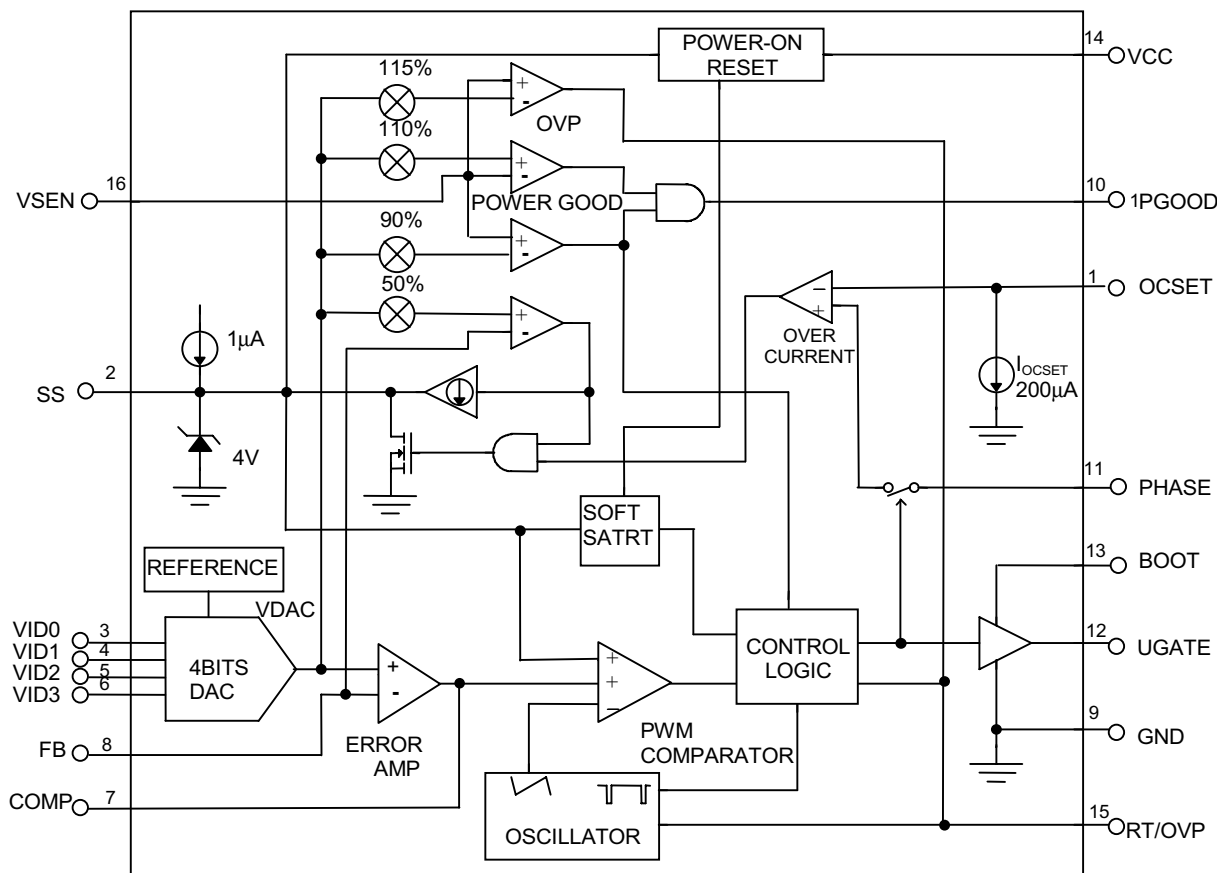
■ TEST CIRCUIT

Refer to TYPICAL APPLICATION CIRCUIT.

ELECTRICAL CHARACTERISTICS ($V_{CC}=12V$, $T_A=25^{\circ}C$, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
VCC Supply Current						
Nominal Supply	U_{GATE} Open	I_{VCC}		2		mA
Power-On Reset						
V_{CC} Threshold	$V_{OCSET}=4.5V$			7	8.5	V
Rising V_{OCSET} Threshold				1.26		V
Oscillator						
Free Running Frequency	RT Open		170	200	230	KHz
Total Variation	$6K\Omega < R_T < 200K\Omega$		-20		+20	%
Ramp Amplitude	RT Open	ΔV_{OSC}		1.5		V_{P-P}
DAC Output Voltage						
DAC Output Voltage Accuracy			-1.5		+1.5	%
Error Amplifier						
DC Gain				76		dB
Gain-Bandwidth Product		GBW		11		MHz
Slew Rate		SR		6		$V/\mu S$
Gate Driver						
Upper Gate Source		R_{UGATE}		8	12	Ω
Upper Gate Sink		R_{UGATE}		5.5	10	Ω
Protection						
Over-Voltage Trip ($V_{VSEN}/VDAC$)			106	115	125	%
OCSET Current Source	$V_{OCSET} = 4.5VDC$	I_{OCSET}	170	200	230	μA
OVP Sourcing Current	$V_{VSEN} = 5.5V, V_{OVP} = 0V$	I_{OVP}	30			mA
SS Current		I_{SS}		10		μA
SS Sink Current under Current Limit	$V_{VSEN} = VDAC, V_{OCSET} = 5.0V,$ $V_{PHASE} = 0V, V_{FB} = VDAC - 50mV$			130		μA
SS Sink Current under Hard Current Limit	$V_{VSEN} = 0, V_{OCSET} = 5.0V,$ $V_{PHASE} = 0V, V_{FB} = 0V$			65		mA
Power Good						
Upper Threshold ($V_{VSEN}/VDAC$)	V_{VSEN} rising		106		114	%
Lower Threshold ($V_{VSEN}/VDAC$)	V_{VSEN} falling		84		94	%
Hysteresis ($V_{VSEN}/VDAC$)	Upper and lower threshold			2		%
PGOOD Voltage Low	$I_{PGOOD} = 5mA$	V_{PGOOD}		0.5		V

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

PIN 1: OCSET - Current limit sense pin. Connect a resistor R_{OCSET} from this pin to the drain of the external MOSFET. R_{OCSET} , an internal $200\mu A$ current source (I_{OCSET}), and the external MOSFET on-resistance ($R_{DS(ON)}$) jointly set the over current trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

If FB pin voltage is sensed to be below 50% of the internal voltage reference VDAC, the over current comparator cycles the soft-start function.

PIN 2: SS - Soft start pin. Connect a

capacitor from this pin to ground. An internal $10\mu A$ current source provides soft start function for the converter.

PIN 3: VID0
PIN 4: VID1
PIN 5: VID2
PIN 6: VID3

- 4-bit DAC voltage select pin. TTL inputs used to set the internal voltage reference VDAC. When left open, these pins are internally pulled up to 5V and provide logic ones. The level of VDAC sets the converter output voltage as well as the PGOOD and OVP thresholds.

Table 1 specifies the VDAC voltage for the 16 combinations of DAC inputs.

Table 1. Output Voltage Program

VID0	VID1	VID2	VID3	VDAC
0	0	0	0	3.5V
1	0	0	0	3.4V
0	1	0	0	3.3V
1	1	0	0	3.2V
0	0	1	0	3.1V
1	0	1	0	3.0V
0	1	1	0	2.9V
1	1	1	0	2.8V
0	0	0	1	2.7V
1	0	0	1	2.6V
0	1	0	1	2.5V
1	1	0	1	2.4V
0	0	1	1	2.3V
1	0	1	1	2.2V
0	1	1	1	2.1V
1	1	1	1	2.0V

PIN 7: COMP - External compensation pin. This pin is connected to error amplifier output and PWM comparator. An RC network is connected to FB pin to compensate the voltage-control feedback loop of the converter.

PIN 8: FB - The error amplifier inverting input pin. The FB pin and COMP pin are used to compensate the voltage-control feedback loop.

PIN 9: GND - Signal GND. It also serves as the power GND for the upper gate driver.

PIN 10: PGOOD-Power good indicator pin. PGOOD is an open drain output. This pin is pulled low when the converter output is $\pm 10\%$ out of the VDAC reference voltage.

PIN 11: PHASE - Over current detection pin. Connect the PHASE pin to source of the external MOSFET. This pin detects the voltage drop across the MOSFET $R_{DS(ON)}$ for over-current protection.

PIN 12: UGATE- External MOSFET gate drive pin. Connect this pin to gate of the external MOSFET.

PIN 13: BOOT - External MOSFET driver power supply pin. To convert 5V main power to V_{CORE} power by driving N-channel MOSFET, supply voltage of no higher than 12V is recommended since the negative power terminal of the internal driver is internally tied to GND.

PIN 14: VCC - The chip power supply pin. Recommended supply voltage is 12V.

PIN 15: RT/OVP- Frequency adjustment and overvoltage indicator pin. This pin is multiplexed to provide two functions. The first function is oscillator switching frequency adjustment. Connecting a resistor (R_T) from this pin to GND increases the frequency according to the following equation:

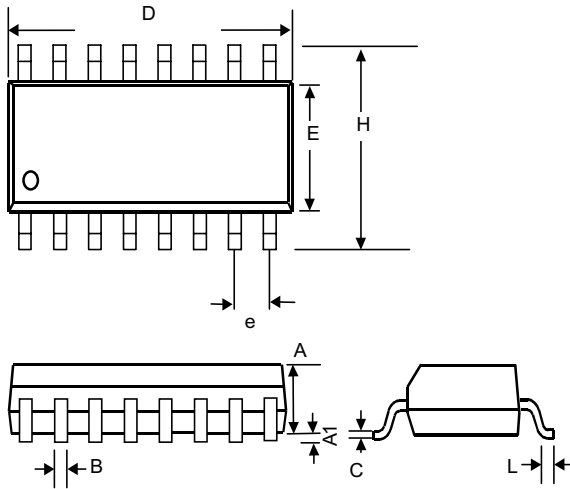
$$F_s \cong 200\text{KHz} + \frac{5 \times 10^5}{\log R_T}$$

The second function for this pin is to drive an external SCR in the event of an over voltage fault.

PIN 16: VSEN - Converter output voltage sense pin. Connect this pin to the converter output. The PGOOD and OVP comparator circuits use this signal to report output voltage status and perform overvoltage protection function.

■ PHYSICAL DIMENSION

- 16 LEAD PLASTIC SO (150 mil) (unit: mm)



SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 (TYP)	
H	5.80	6.20
L	0.40	1.27

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