
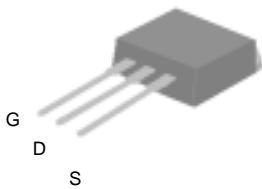


# N-channel Enhancement-mode Power MOSFET

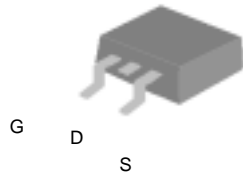
## PRODUCT SUMMARY

$BV_{DSS}$	80V
$R_{DS(ON)}$	45m $\Omega$
$I_D$	21A

 **Pb-free; RoHS-compliant TO-251 (IPAK) and TO-252 (DPAK)**



TO-251 (suffix J)



TO-252 (suffix H)

## DESCRIPTION

The SSM9980Gx achieves fast switching performance with low gate charge without a complex drive circuit. It is suitable for low voltage applications such as DC/DC converters and general load-switching circuits.

The SSM9980GH is in a TO-252 package, which is widely used for commercial and industrial surface-mount applications.

The through-hole version, the SSM9980GJ in TO-251, is available for vertical mounting, where a small footprint is required on the board, and/or an external heatsink is to be attached.

These devices are manufactured with an advanced process, providing improved on-resistance and switching performance.

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-source voltage	80	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Continuous drain current, $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	21	A
		13.4	A
$I_{DM}$	Pulsed drain current <sup>1</sup>	80	A
$P_D$	Total power dissipation, $T_C = 25^\circ\text{C}$	41	W
	Linear derating factor	0.33	W/ $^\circ\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Maximum thermal resistance, junction-case	3.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum thermal resistance, junction-ambient	110	$^\circ\text{C}/\text{W}$

### Notes:

1. Pulse width must be limited to avoid exceeding the safe operating area.

**ELECTRICAL CHARACTERISTICS** (at  $T_j = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown voltage temperature coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	-	0.07	-	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static drain-source on-resistance	$V_{GS}=10V, I_D=12A$	-	-	45	m $\Omega$
		$V_{GS}=4.5V, I_D=8A$	-	-	55	m $\Omega$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$	Forward transconductance	$V_{DS}=5V, I_D=12A$	-	20	-	S
$I_{DSS}$	Drain-source leakage current	$V_{DS}=80V, V_{GS}=0V$	-	-	10	$\mu A$
		$V_{DS}=64V, V_{GS}=0V, T_j = 150^\circ\text{C}$	-	-	100	$\mu A$
$I_{GSS}$	Gate-source leakage current	$V_{GS}=\pm 25V$	-	-	$\pm 100$	nA
$Q_g$	Total gate charge <sup>2</sup>	$I_D=12A$	-	18	30	nC
$Q_{gs}$	Gate-source charge	$V_{DS}=64V$	-	5	-	nC
$Q_{gd}$	Gate-drain ("Miller") charge	$V_{GS}=4.5V$	-	11	-	nC
$t_{d(on)}$	Turn-on delay time <sup>2</sup>	$V_{DS}=40V$	-	11	-	ns
$t_r$	Rise time	$I_D=12A$	-	20	-	ns
$t_{d(off)}$	Turn-off delay time	$R_G=3.3\Omega, V_{GS}=10V$	-	29	-	ns
$t_f$	Fall time	$R_D=3.3\Omega$	-	30	-	ns
$C_{iss}$	Input capacitance	$V_{GS}=0V$	-	1810	2900	pF
$C_{oss}$	Output capacitance	$V_{DS}=25V$	-	135	-	pF
$C_{rss}$	Reverse transfer capacitance	$f=1.0\text{MHz}$	-	96	-	pF
$R_g$	Gate resistance	$f=1.0\text{MHz}$		1.6		$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward voltage <sup>2</sup>	$I_S=20A, V_{GS}=0V$	-	-	1.2	V
$t_{rr}$	Reverse-recovery time <sup>2</sup>	$I_S=12A, V_{GS}=0V,$	-	57	-	ns
$Q_{rr}$	Reverse-recovery charge	$dI/dt=100A/\mu s$	-	140	-	nC

**Notes:**

1. Pulse width must be limited to avoid exceeding the maximum junction temperature of  $150^\circ\text{C}$ .

2. Pulse width  $<300\mu s$ , duty cycle  $<2\%$ .

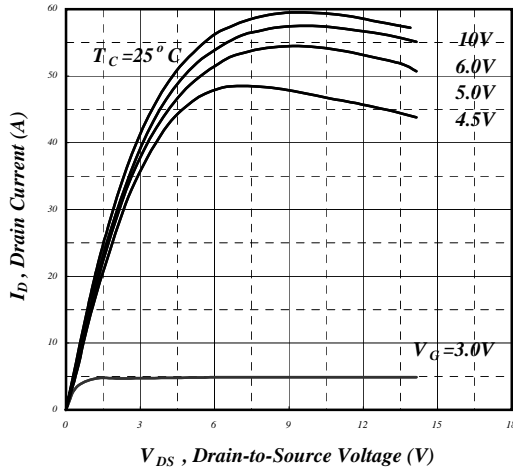


Fig 1. Typical Output Characteristics

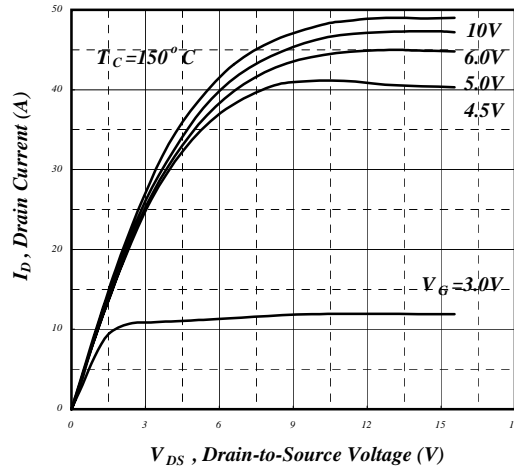


Fig 2. Typical Output Characteristics

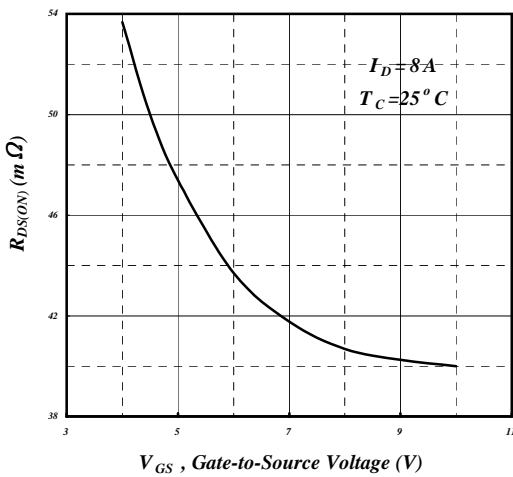


Fig 3. On-Resistance vs. Gate Voltage

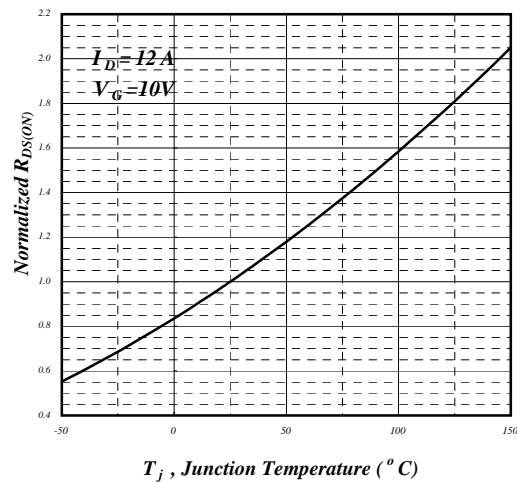


Fig 4. Normalized On-Resistance vs. Junction Temperature

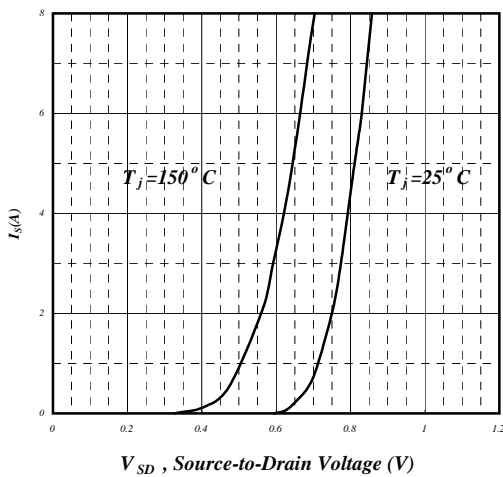


Fig 5. Forward Characteristic of Reverse Diode

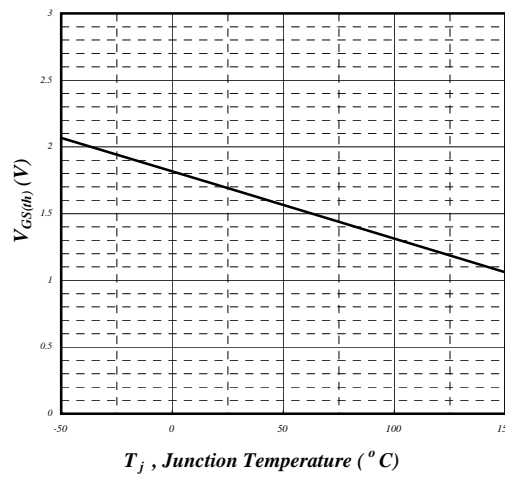


Fig 6. Gate Threshold Voltage vs. Junction Temperature

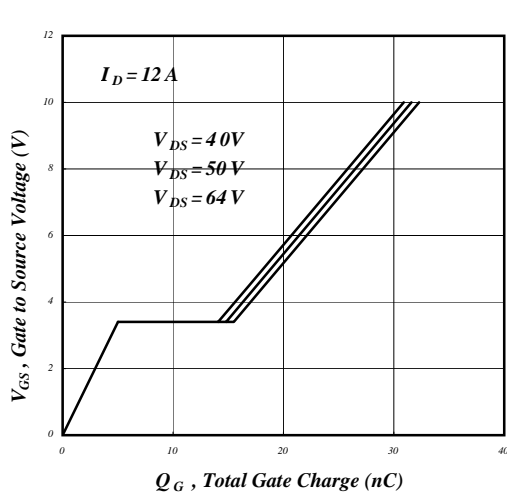


Fig 7. Gate Charge Characteristics

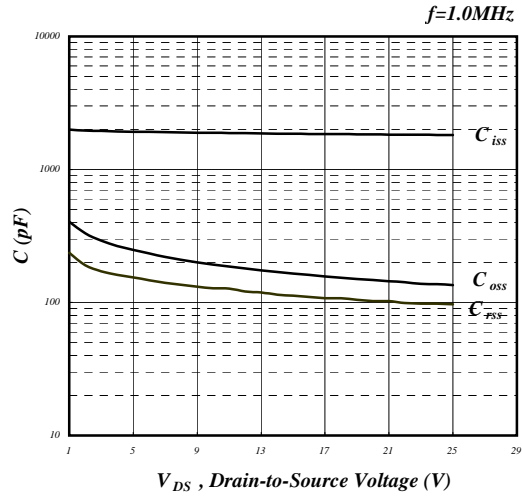


Fig 8. Typical Capacitance Characteristics

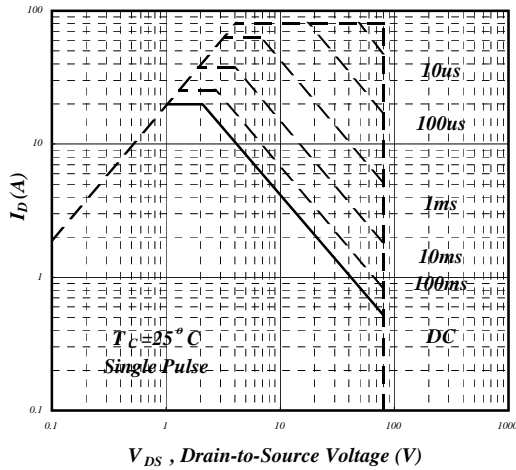


Fig 9. Maximum Safe Operating Area

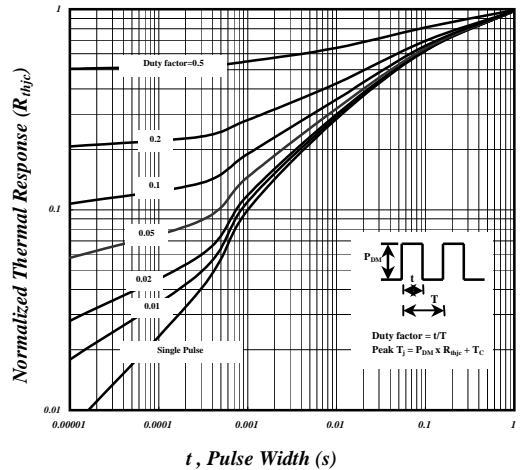


Fig 10. Effective Transient Thermal Impedance

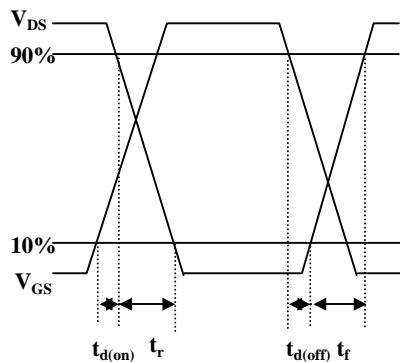


Fig 11. Switching Time Waveform

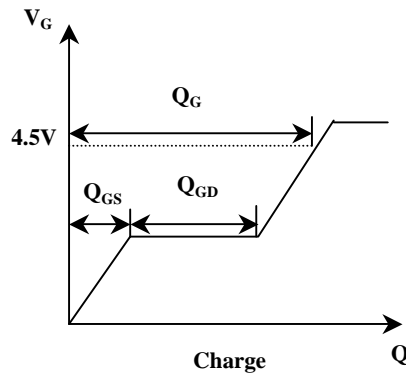
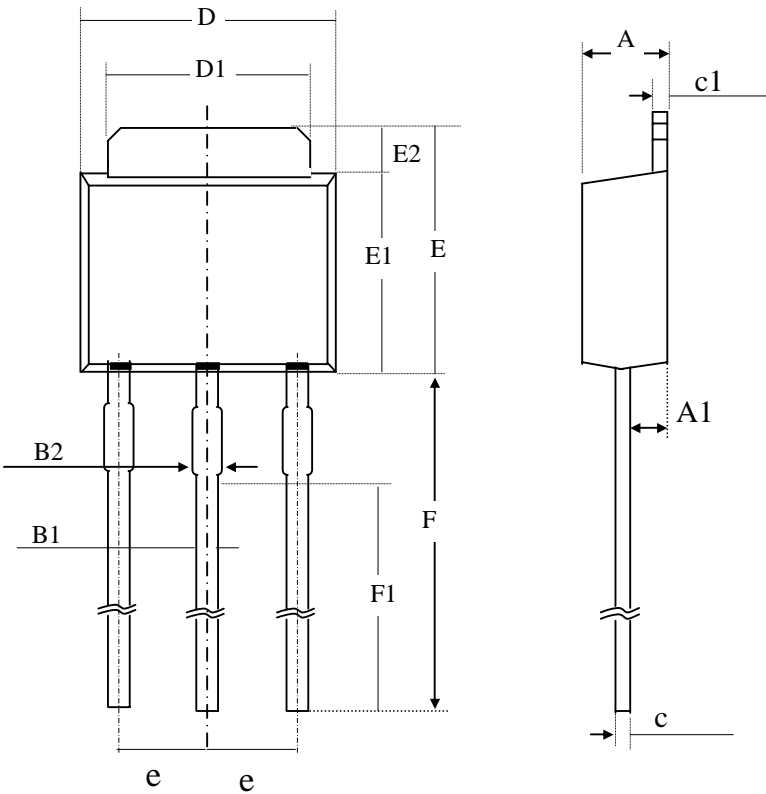


Fig 12. Gate Charge Waveform

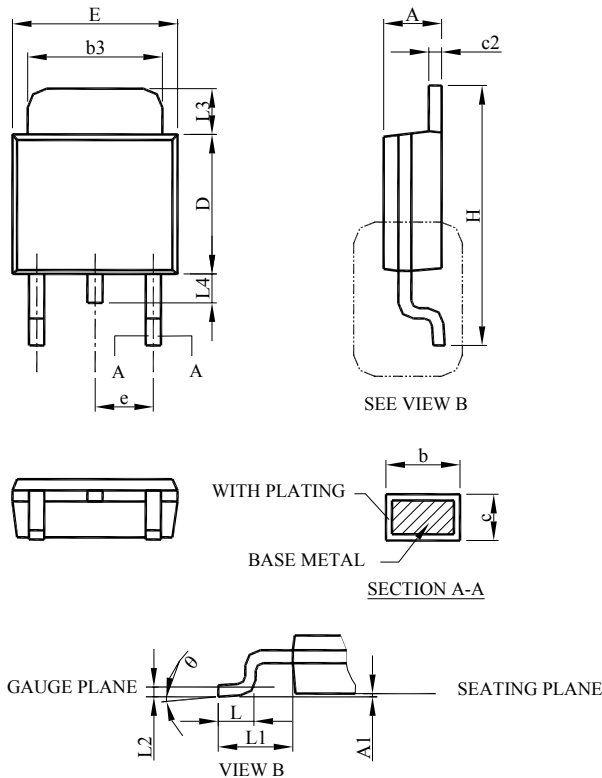
## PHYSICAL DIMENSIONS: TO-251 (I-PAK)



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.90	1.20	1.50
B1	0.50	0.60	0.70
B2	0.60	0.72	0.90
c	0.45	0.50	0.60
c1	0.45	0.50	0.55
D	6.40	6.60	6.80
D1	5.20	5.35	5.50
E	6.80	7.00	7.20
E1	5.40	5.60	5.80
E2	1.40	1.50	1.60
e	--	2.30	--
F	7.20	7.50	7.80
F1	1.50	1.60	1.80

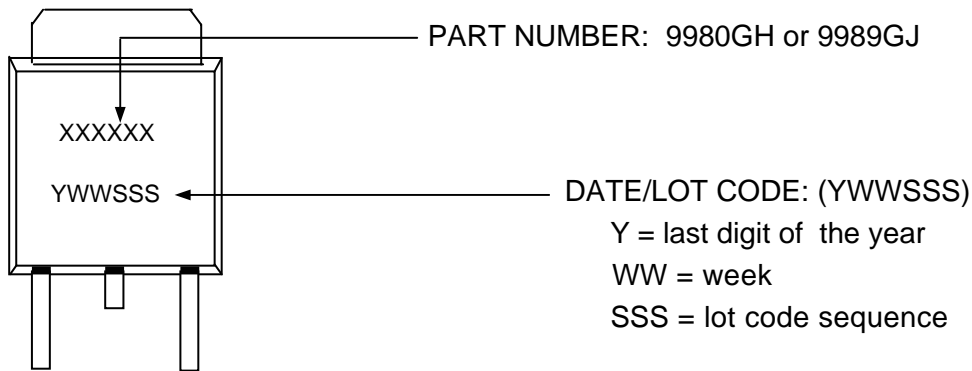
1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

## PHYSICAL DIMENSIONS: TO-252 (D-PAK)



SYMBOL	TO-252-3L	
	MILLIMETERS	
	MIN.	MAX.
A	1.80	2.80
A1	0.00	0.13
b	0.40	1.00
b3	4.80	5.90
c	0.35	0.65
c2	0.40	0.89
D	5.10	6.30
E	6.00	7.00
e	2.30 BSC	
H	7.80	11.05
L	1.00	2.55
L1	2.20	3.05
L2	0.35	0.65
L3	0.50	2.03
L4	0.50	1.20
θ	0°	8°

## PART MARKING



## PACKING: Moisture sensitivity level MSL3

TO-252: 3000 pcs in antistatic tape on a reel packed inside a moisture barrier bag (MBB).

TO-251: 1000pcs in tubes packed inside a moisture barrier bag (MBB).

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, express or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.