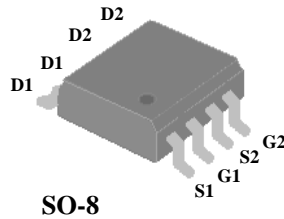


N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

PRODUCT SUMMARY

Simple Drive Requirement
Low Gate Charge
Fast Switching Performance

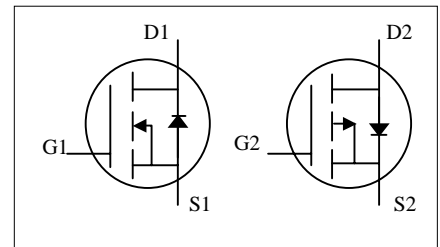


N-CH	BV_{DSS}	20V
	$R_{DS(ON)}$	18m Ω
	I_D	8.3A
P-CH	BV_{DSS}	-20V
	$R_{DS(ON)}$	45m Ω
	I_D	-5A

DESCRIPTION

The advanced power MOSFETs from Silicon Standard Corp. provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 12	± 12	V
$I_D@T_A=25^\circ C$	Continuous Drain Current ³	8.3	-5	A
$I_D@T_A=70^\circ C$	Continuous Drain Current ³	6.5	-4	A
I_{DM}	Pulsed Drain Current ¹	30	-20	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/ $^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ C$

THERMAL DATA

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	62.5	$^\circ C/W$

N-CH Electrical Characteristics @ $T_J=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=9A$	-	-	16	m Ω
		$V_{GS}=4.5V, I_D=8.3A$	-	-	18	m Ω
		$V_{GS}=2.5V, I_D=5.2A$	-	-	30	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	-	-	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=8.3A$	-	8.3	-	S
I_{DSS}	Drain-Source Leakage Current ($T_J=25^{\circ}\text{C}$)	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current ($T_J=70^{\circ}\text{C}$)	$V_{DS}=16V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 12V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=8A$	-	22	-	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=16V$	-	3	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	9	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=10V$	-	11	-	ns
t_r	Rise Time	$I_D=1A$	-	13	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=5V$	-	30	-	ns
t_f	Fall Time	$R_D=10\Omega$	-	14	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1350	-	pF
C_{oss}	Output Capacitance	$V_{DS}=20V$	-	325	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	255	-	pF

SOURCE-DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=1.8A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time ²	$I_S=8A, V_{GS}=0V,$	-	32	-	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	24	-	nC

P-CH Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-6A$	-	-	40	$m\Omega$
		$V_{GS}=-4.5V, I_D=-5A$	-	-	45	$m\Omega$
		$V_{GS}=-2.5V, I_D=-4A$	-	-	80	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5	-	-	V
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-2.2A$	-	2.2	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^{\circ}\text{C}$)	$V_{DS}=-20V, V_{GS}=0V$	-	-	-1	μA
	Drain-Source Leakage Current ($T_j=70^{\circ}\text{C}$)	$V_{DS}=-16V, V_{GS}=0V$	-	-	-25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 12V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=-5A$	-	13	-	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-16V$	-	1.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	4.5	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=-10V$	-	8	-	ns
t_r	Rise Time	$I_D=-1A$	-	17	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=-5V$	-	24	-	ns
t_f	Fall Time	$R_D=10\Omega$	-	36	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	920	-	pF
C_{oss}	Output Capacitance	$V_{DS}=-20V$	-	90	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	85	-	pF

SOURCE-DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	30
V_{SD}	Forward On Voltage ²	$I_S=-1.8A, V_{GS}=0V$	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	$I_S=-5A, V_{GS}=0V,$	-	28	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	16	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board ; 135 °C/W when mounted on Min. copper pad.

THIS PRODUCT IS AN ELECTROSTATIC SENSITIVE, PLEASE HANDLE WITH CAUTION.

THIS PRODUCT HAS BEEN QUALIFIED FOR CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENT IN LIFE SUPPORT DEVICE OR SYSTEM ARE NOT AUTHORIZED.

N-Channel

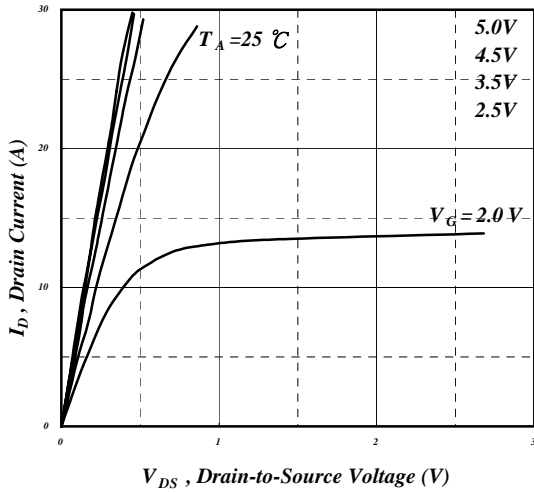


Fig 1. Typical Output Characteristics

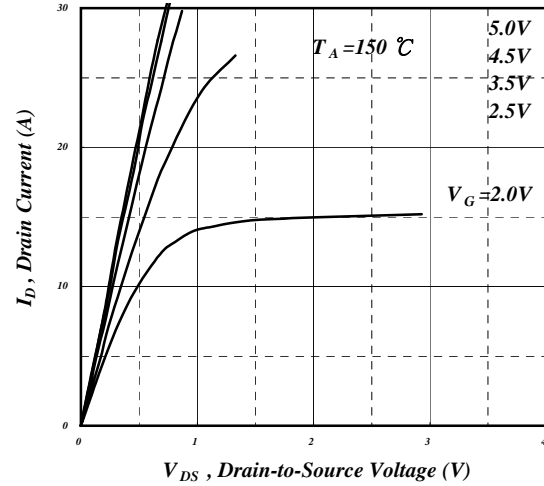


Fig 2. Typical Output Characteristics

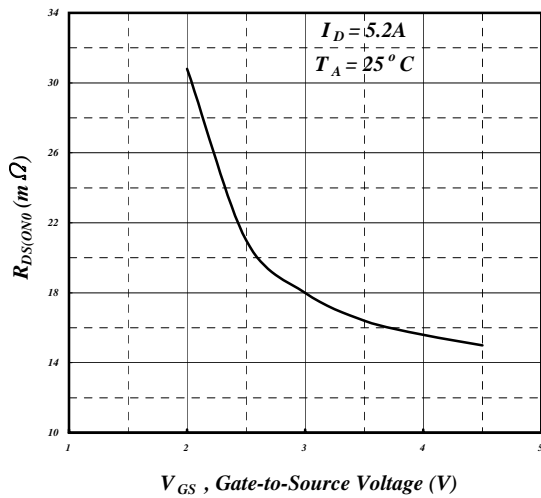


Fig 3. On-Resistance v.s. Gate Voltage

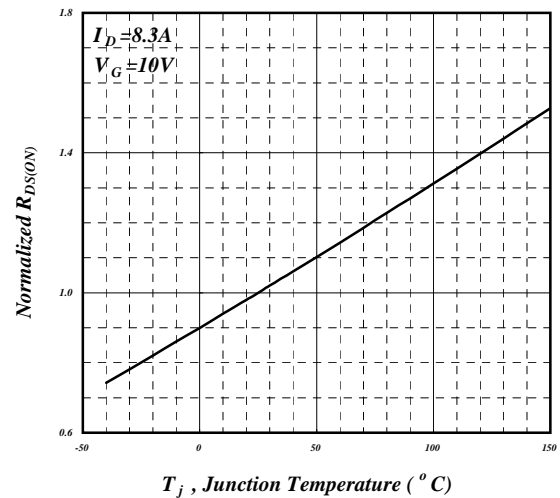


Fig 4. Normalized On-Resistance v.s. Junction Temperature

N-Channel

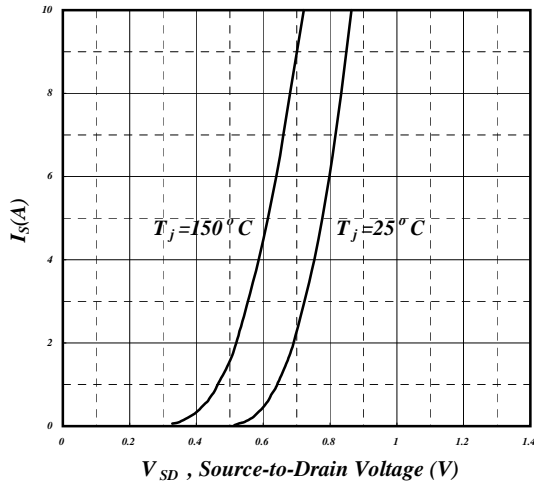


Fig 5. Forward Characteristic of Reverse Diode

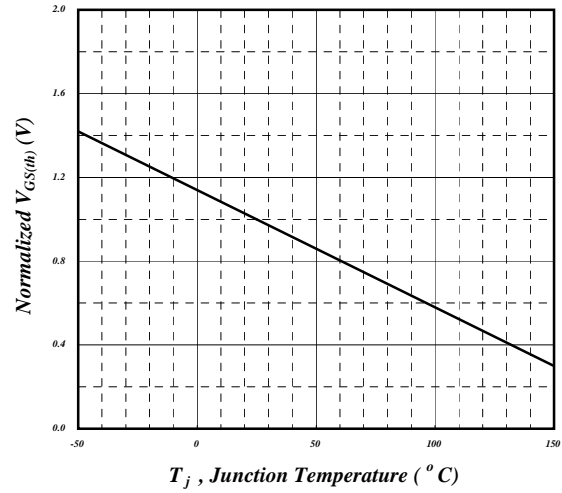


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

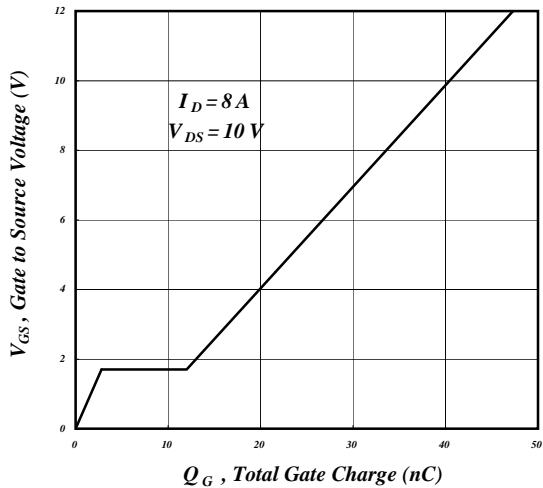


Fig 7. Gate Charge Characteristics

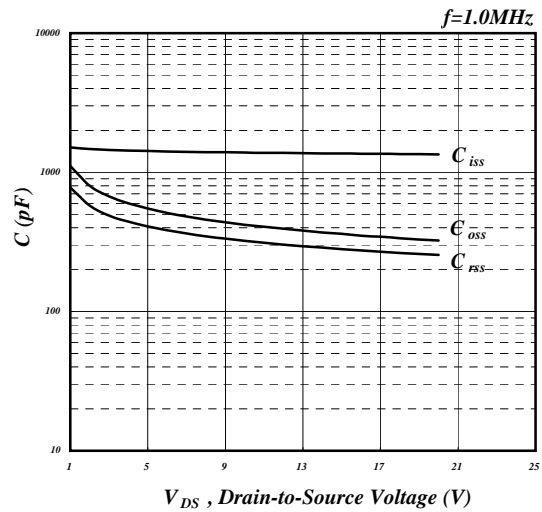


Fig 8. Typical Capacitance Characteristics

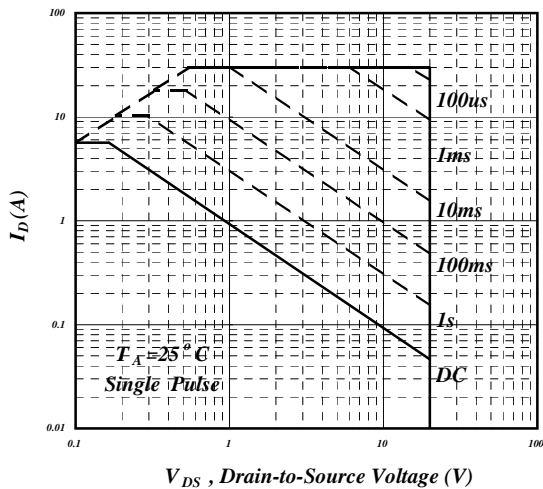


Fig 9. Maximum Safe Operating Area

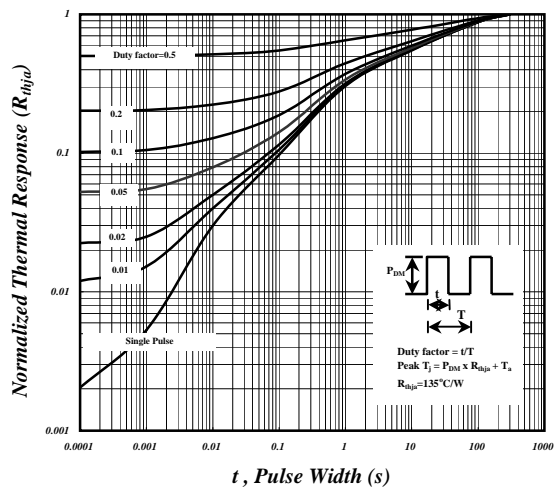


Fig 10. Effective Transient Thermal Impedance

N-Channel

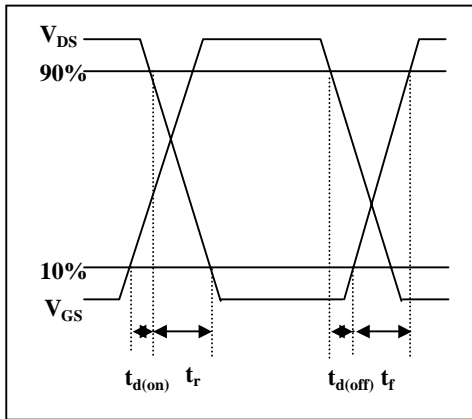


Fig 11. Switching Time Waveform

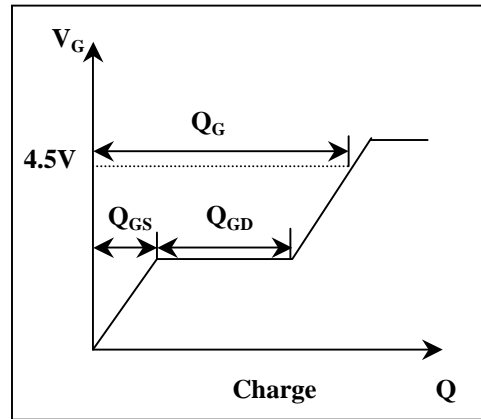


Fig 12. Gate Charge Waveform

P-Channel

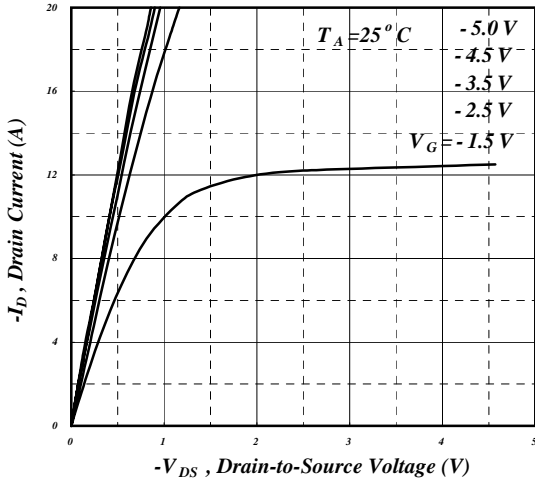


Fig 1. Typical Output Characteristics

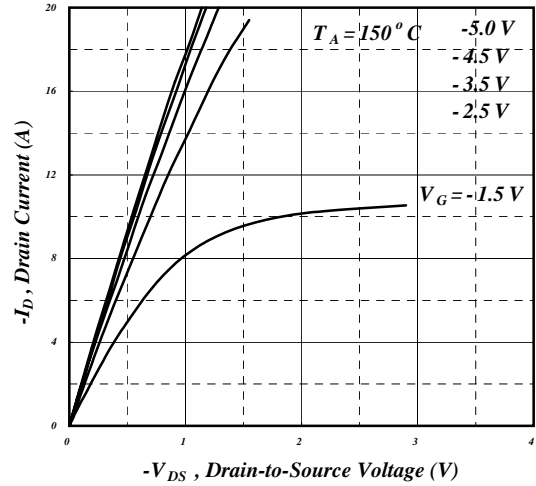


Fig 2. Typical Output Characteristics

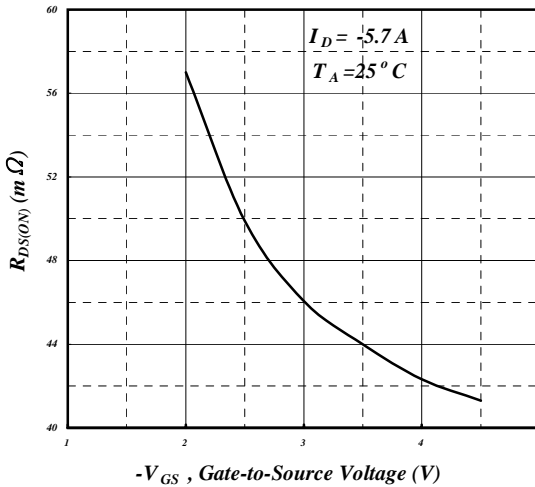


Fig 3. On-Resistance v.s. Gate Voltage

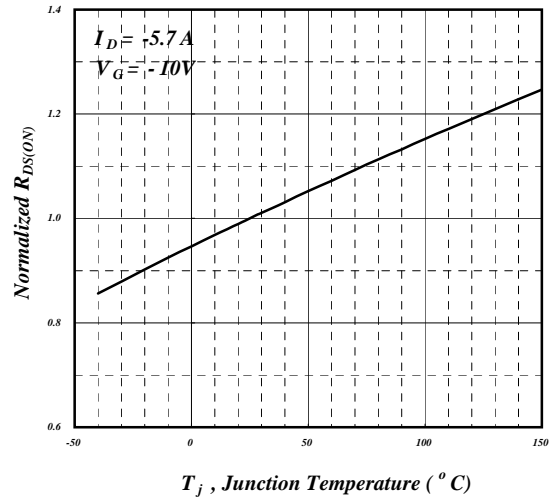


Fig 4. Normalized On-Resistance v.s. Junction Temperature

P-Channel

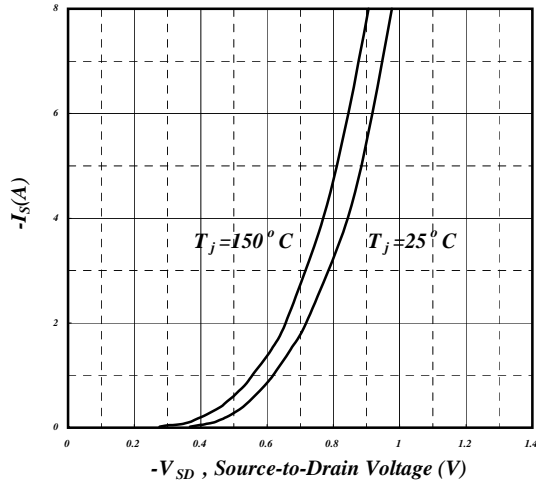


Fig 5. Forward Characteristic of Reverse Diode

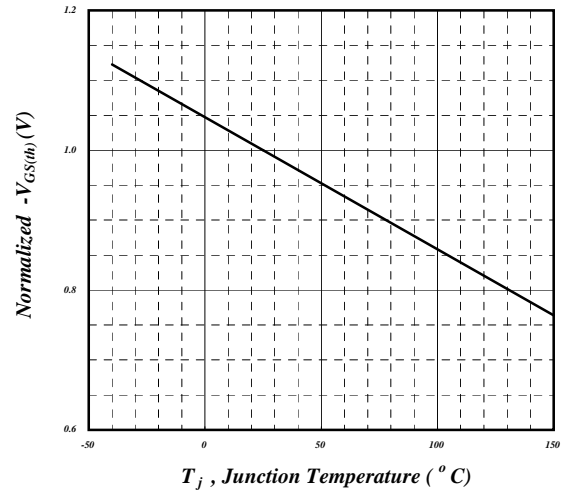


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

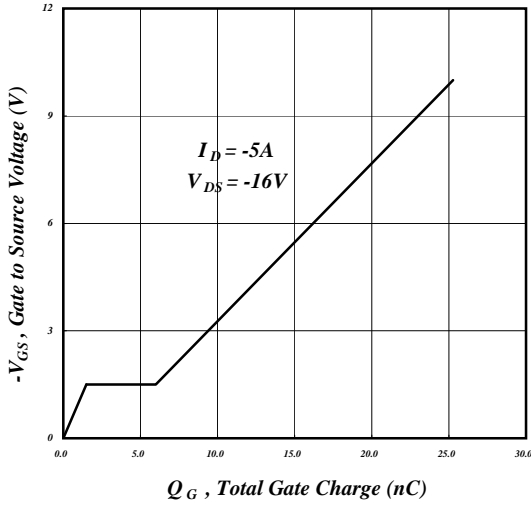


Fig 7. Gate Charge Characteristics

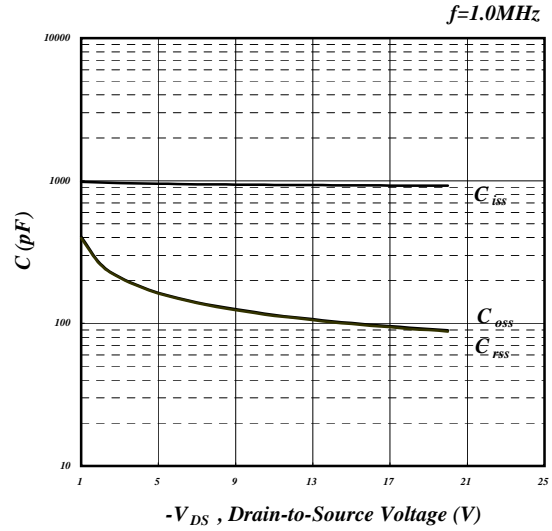


Fig 8. Typical Capacitance Characteristics

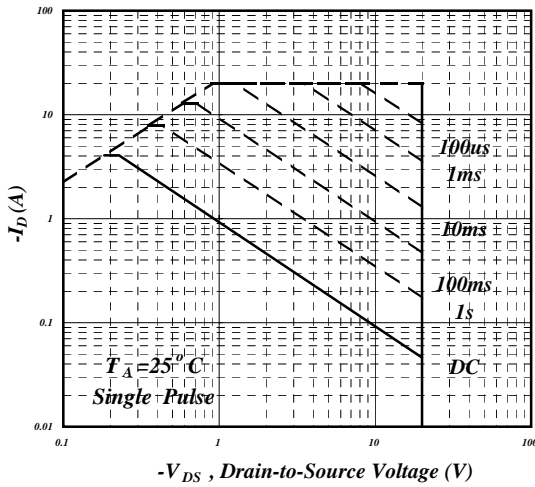


Fig 9. Maximum Safe Operating Area

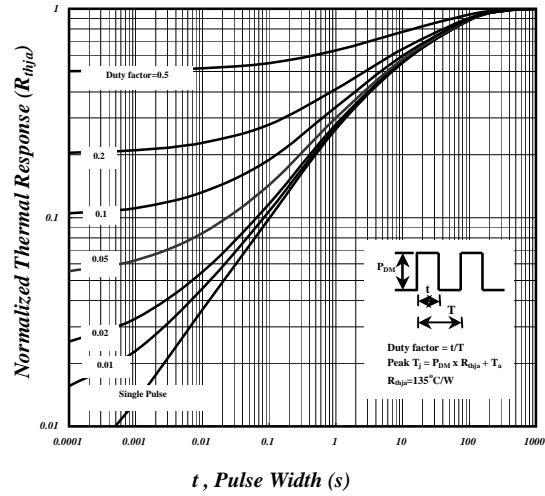


Fig 10. Effective Transient Thermal Impedance

P-Channel

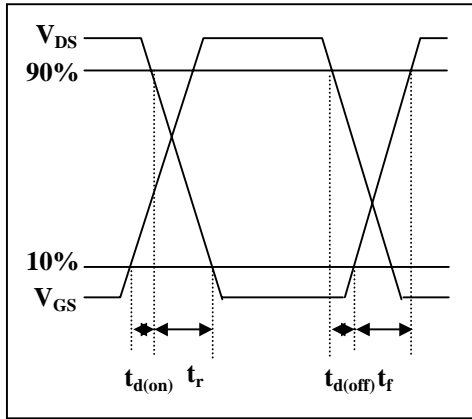


Fig 11. Switching Time Waveform

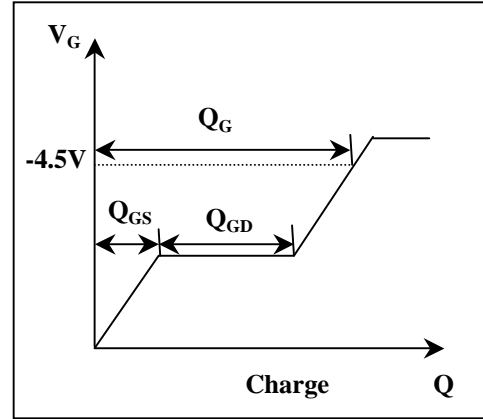
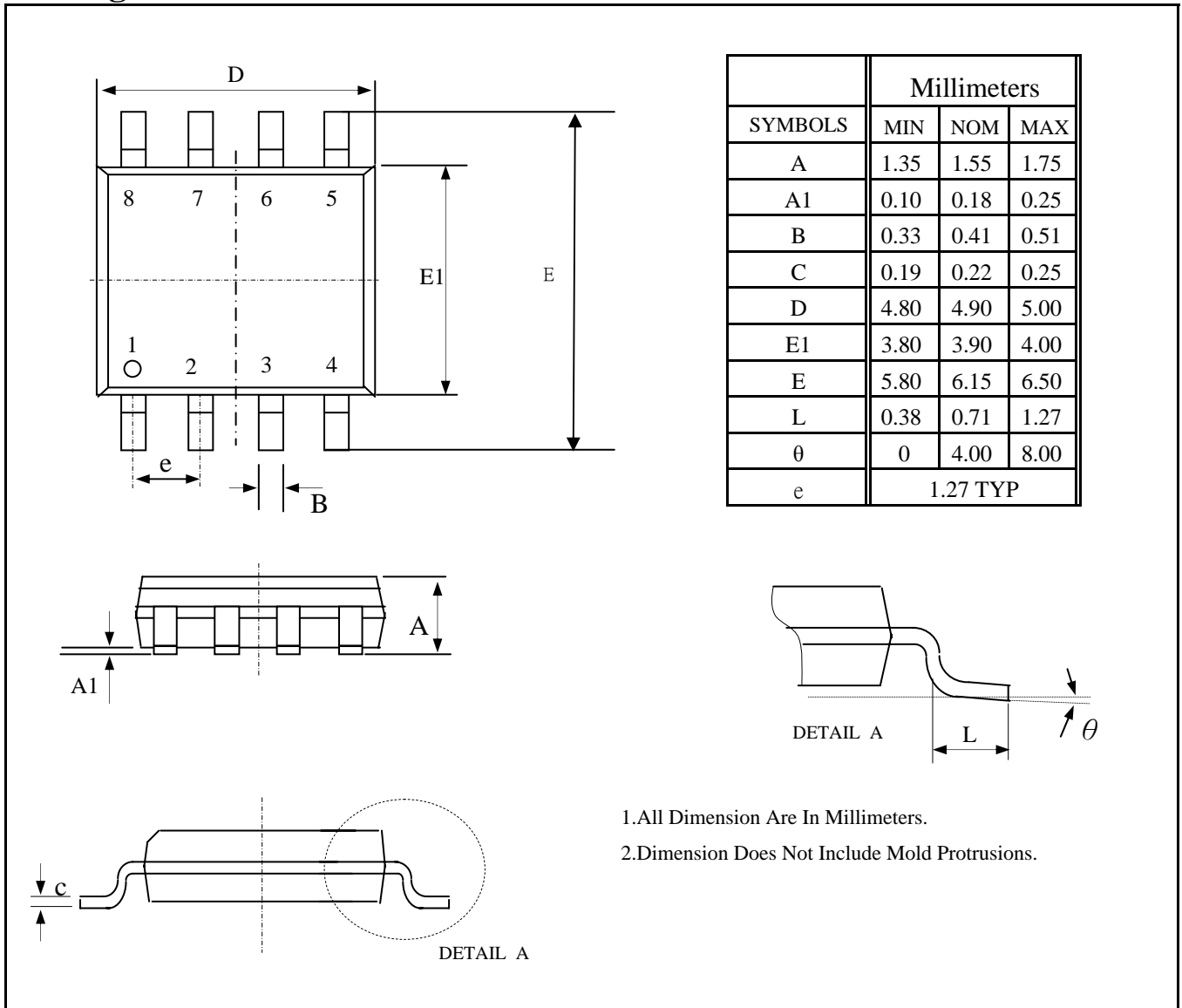
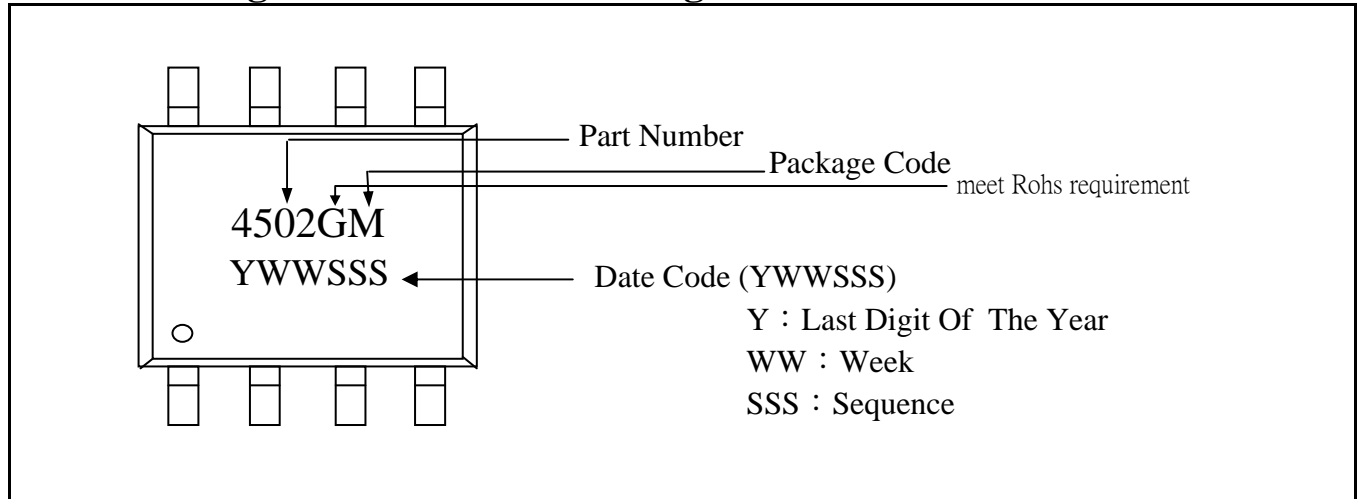


Fig 12. Gate Charge Waveform

Package Outline : SO-8



Part Marking Information & Packing : SO-8



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